CLAIMS

What is claimed is:

1. A NOR array comprising:

a first plurality of word lines, each word line connecting to the gates of a row of nitride read only memory (NROM) cells;

a second plurality of bit lines, each bit line connecting to one diffusion area of each NROM cell in a column of said NROM cells; and

a third plurality of common lines, each common line connecting to the other diffusion areas of each NROM cell in a row of said NROM cells.

2. An array according to claim 1 wherein each said NROM cell has a common line storage area and a bit line storage area.

3. An array according to claim 2 wherein said bit line storage area stores at least one electrically erasable programmable read only memory (EEPROM) bit and said common line storage area stores at least one FLASH EEPROM bit.

4. An array according to claim 2 wherein said common line and bit line storage areas store FLASH EEPROM bits.

5. An array according to claim 4 and wherein the bits stored in the bit line storage areas of cells on a bit line are erasable together.

6. An array according to claim 4 and wherein the bits stored in the common line storage areas of cells of a common line are erasable together.

7. An array according to claim 2 and also comprising a sensing unit having a CL sense amplifier and a BL sense amplifier.

8. An array according to claim 7 and wherein said BL sense amplifier is a close to ground sense amplifier.

9. An array according to claim 7 and wherein said CL sense amplifier is a non-close to ground sense amplifier.

10. An array according to claim 7 wherein each said common line storage area is on a common line side of said cell which is connectable to said CL sense amplifier and each said bit line storage area is on a bit line side of said cell which is connectable to said BL sense amplifier.

11. An array according to claim 1 wherein each said NROM cell has at least one EEPROM storage area.

12. An array according to claim 11 and wherein said at least one EEPROM storage area is a bit line storage area and the EEPROM bits stored in the bit line storage areas of cells sharing the same bit line can be individually erased.

13. An array according to claim 11 and wherein said at least one EEPROM storage area is a bit line storage area and wherein a subset of the EEPROM bits stored in the bit line storage areas of cells sharing the same bit line can be erased together.

14. An array according to claim 11 wherein each said EEPROM storage area is on a bit line side of said cell and wherein said bit line side is connectable to a close to ground sense amplifier.

15. A memory array comprising:

a plurality of memory cells each capable of storing at least one EEPROM bit and at least one FLASH EEPROM bit.

16. A memory array comprising:

a first plurality of memory cells each capable of storing at least one EEPROM bit; and

a second plurality of select transistors each of which select a group of more than one of said memory cells.

17. A method comprising:

having a plurality of memory cells in a NOR memory array, wherein each said cell has bit line and common line storage areas, wherein said bit line storage areas area connected to one of a second plurality of bit lines and wherein said common line storage areas are connected to one of a third plurality of common lines;

reading said bit line storage areas with a close to ground sense amplifier; and

reading said common line storage areas with a non-close to ground sense amplifier.

18. A method according to claim 17 and also comprising erasing a group of said common line storage areas together.

19. A method according to claim 17 and also comprising erasing a group of said bit line storage areas together.

20. A method according to claim 17 and also comprising erasing said bit line storage areas individually.

21. A method comprising:

having a plurality of memory cells in a NOR memory array, wherein each memory cell has one storage area connected to one of a second plurality of bit lines; and

reading said bit line storage areas with a sense amplifier that has a close to ground input level.

22. A method according to claim 21 and also comprising erasing said storage areas individually.

23. A method according to claim 21 and also comprising erasing a group of said bit line storage areas together.